1. A method of making semiconductor device packages, comprising:
forming a layered assembly by attaching a wafer to a dielectric layer;
subsequently, testing semiconductor devices in said wafer; and
subsequently, dicing said layered assembly.

sub B1

2. The method of claim 1, further comprising the step of connecting said semiconductor devices to input/output devices on the dielectric layer.

3. The method of claim 2, wherein said testing is conducted through said input/output devices.

4. The method of claim 3, further comprising the step of discarding one or more defective packages.

5. The method of claim 1, wherein said step of forming said layered assembly includes the step of adhering said wafer to said dielectric layer.

6. The method of claim 5, further comprising the step of electrically connecting said semiconductor devices to ball grid arrays on said dielectric layer.

7. The method of claim 6, wherein said connecting step comprises the step of locating wire bonds in openings through said dielectric layer.

8. The method of claim 6, wherein said connecting step comprises the step of connecting solder bumps on said wafer to circuit traces on said dielectric layer.

9. The method of claim 6, wherein said dicing step is performed by a saw.

10. The method of claim 6, further comprising the step of providing a metal layer in said layered assembly.

Sub A1

11. A method of making semiconductor device packages, comprising:

forming a layered assembly by attaching a semiconductor wafer and a metal layer to a dielectric layer;

connecting semiconductor devices in said semiconductor wafer to ball grid arrays on said dielectric layer; and

subsequently, dicing said layered assembly.

Sub B1

12. The method of claim 11, wherein said forming step comprises the step of adhering said wafer to said metal layer.

13. The method of claim 11, wherein said connecting step comprises the step of locating wire bonds in openings in said dielectric layer.

14. The method of claim 13, further comprising the step of connecting said wire bonds to conductive traces on said dielectric layer.

15. The method of claim 11, wherein said connecting step comprises the step of connecting solder bumps on said wafer to conductive traces on said dielectric layer.

16. The method of claim 15, further comprising the step of connecting said traces to conductive vias extending through said dielectric layer.

17. The method of claim 11, wherein said dicing step is performed by a saw.

18. The method of claim 11, further comprising the step of testing said semiconductor devices through said ball grid arrays.

B' cont'd

19. A method of making semiconductor device packages, comprising:

aligning a semiconductor wafer with respect to a dielectric tape;

subsequently, connecting semiconductor devices in said wafer to ball grid arrays on said dielectric tape; and

simultaneously dicing said wafer and said dielectric tape.

20. The method of claim 19, wherein said wafer is optically aligned with respect to said dielectric tape.

21. The method of claim 19, wherein said wafer is magnetically aligned with respect to said dielectric tape.

22. The method of claim 21, wherein oppositely charged magnetic elements are provided on said wafer and said tape.

23. The method of claim 21, further comprising the step of locating a magnetic ring in a charged slot.

24. A semiconductor device package, comprising:

a semiconductor device having edges formed by a dicing operation;

a dielectric substrate having edges formed by said dicing operation;

a ball grid array on said dielectric substrate, said substrate being located between said semiconductor device and said ball grid array; and

electrical connections between said semiconductor device and said ball grid array.

25. The package of claim 24, further comprising a metal layer having edges formed by said dicing operation.

26. The package of claim 25, wherein said metal layer provides a ground plane for said electrical connections.

27. The package of claim 26, wherein said semiconductor device is located between said metal layer and said dielectric substrate.

28. The package of claim 25, wherein said metal layer is arranged to dissipate heat from said semiconductor device.

29. The package of claim 25, wherein said metal layer comprises copper.

30. The package of claim 25, wherein said connections comprise wire bonds.

31. The package of claim 25, wherein said connections comprise conductive vias.

32. The package of claim 31, wherein said connections further comprise conductive traces on opposite sides of said substrate.

33. The package of claim 32, further comprising solder bumps on said semiconductor device, said bumps being connected to said traces.

34. The package of claim 24, further comprising an insulative solder mask for covering said dielectric substrate.

sb B1 35. A method of handling a plurality of semiconductor devices arrayed in a semiconductor wafer, comprising:

adhering said wafer to a flexible substrate;

connecting said semiconductor devices to respective ball grid arrays located on said flexible substrate; and

testing said semiconductor devices through said ball grid arrays.

36. The method of claim 35, further comprising the step of identifying defective packages.

37. The method of claim 35, further comprising the step of singulating packages from said wafer and said substrate.

38. The method of claim 37, further comprising the step of segregating defective packages from other packages.